The Half-Adder Circuit Design and Simulations in 180 nm technology

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***Abstract*—The purpose of this lab is to design a Half-Adder circuit in CMOS 180nm technology to meet the loading condition of 10fF and the rise/fall time of 500ps with the maximum input frequency of 100 MHz. The design of the half-adder is implemented using static complementary logic style with conscious transistor sizing to meet the timing requirements under process and mismatch variations. The Half-adder's functional, monte-carlo and process variations were simulated to realize worst delay, average power and power delay product in Cadence. From the monte-carlo simulations, the average power had the mean of 18.4 uW with stdv. of 273nW; and the worst delay had the mean of 151.5 ps with stdv. of 11.8 ps. The process corner simulation showed that the worst delay, worst power and worst power delay product of 215.9 ps, 19.67 uW and 3.9 fJ were obtained at ss85, ff85 and ss85 corners, respectively.**

I. Introduction

THE two input half-adder circuit is one of the most fundamental blocks of any processors. It basically adds two binary inputs, and outputs *sum* and the *carry* binary data. The task of this lab is to design the half-adder block in cadence given the capacitive loading of 10fF and the timing constraints where rise/fall time should be less than 500 ps. The *sum* output of the half-adder is the XOR result of boolean inputs A and B. The *carry* output of the half-adder is the AND result of boolean inputs A and B.

II. Half-Adder Design Process

A. Logic Style Selection

For the purpose of this lab, the static complementary logic style is chosen for the matter of circuit design and simulation simplicity as there are no strict power constraints nor minimum transistor constraints. Although there are numerous logic styles out there such as dynamic logic, Psudo-NMOS logic and the transmission gate logic to design the combinational logic blocks, the static complementary logic style is the most robust and reliable logic style out of any other logic styles. Thus, the static complementary logic style containing pull-up and pull-down network is selected for this lab as shown in figure **??**.

B. Transistor Sizing and Delay Equalizing Strategy

The standard static complementary pull-up/pull-down sizing strategy was used to sufficiently meet the timing criteria of the output signals with rise/fall time of 500ps for 100 MHz input signal. Only the width of the transistors were changed for this design. The lengths were not changed for any transistors, but kept to minimum. The minimum pull-down base width of 220 nm was enough to meet the design constraints under the process and mismatch variations.

It is known that the PMOS and NMOS differs in the mobility of their majority carriers. One must find the sizing ratio between PMOS and NMOS that equalizes TPHL and TPLH delays. After sweeping the PMOS width while keeping the NMOS transistor width to minimum (220 nm) in an inverter circuit, the PMOS size of 792 nm gave the equalized propagation delays, meaning the PMOS to NMOS ratio of 1:3.6 can be used for the 180nm technology.

All the inverters used in the half-adder design has a minimum NMOS size of 220 nm and PMOS size of 220 nm x 3.6 = 792 nm. For the NAND subcomponent of the AND gate, the two series NMOS were sized with 2 x 220 nm = 440 nm and the two parallel PMOS were sized with 220 nm x 3.6 = 792 nm. For the XOR gate, the two series NMOS were sized to 220 nm x 2 = 440 nm and the two series PMOS were sized to 220 nm x 3.6 x 2 = 1.584 um. The finalized circuit with labeled transistor sizes are shown figure **??**.

Since the timing requirements were very relaxed, it wasn't necessary to upsize the upcoming stages using the path effort optimization strategy; this can make the circuit work faster but at the cost of higher power consumption. Therefore, the minimum possible staging ratio was used to size the transistors.

III. Simulations

The transient simulation was performed by making the input *b* run at 100 MHz and input *a* run at 1/3 of the frequency of *b* to test the circuit with all the possible inputs variations and find the worst case delays which are shown in figure **??**.

The monte-carlo simulation shown in figure **??** with 100 samples at 27°C was performed to evaluate the propagation delay and the average power (avg(i(t))*1.8V) under mismatch variations. It was found that the average power had a mean of 18.4 uW with stdv. of 273nW; and the worst delay had a mean of 151.5 ps with stdv. of 11.8 ps.

From the process corner simulations shown in figure **??**, the worst overall delay of 215.9 ps was obtained during the slow-slow 85°C (ss85) corner. The worst power consumption of 19.67 uW was obtained during the fast-fast 85°C (ff85) corner. Finally, the worst power delay product of 3.9 fJ was obtained at slow-slow 85°C (ss85) corner.

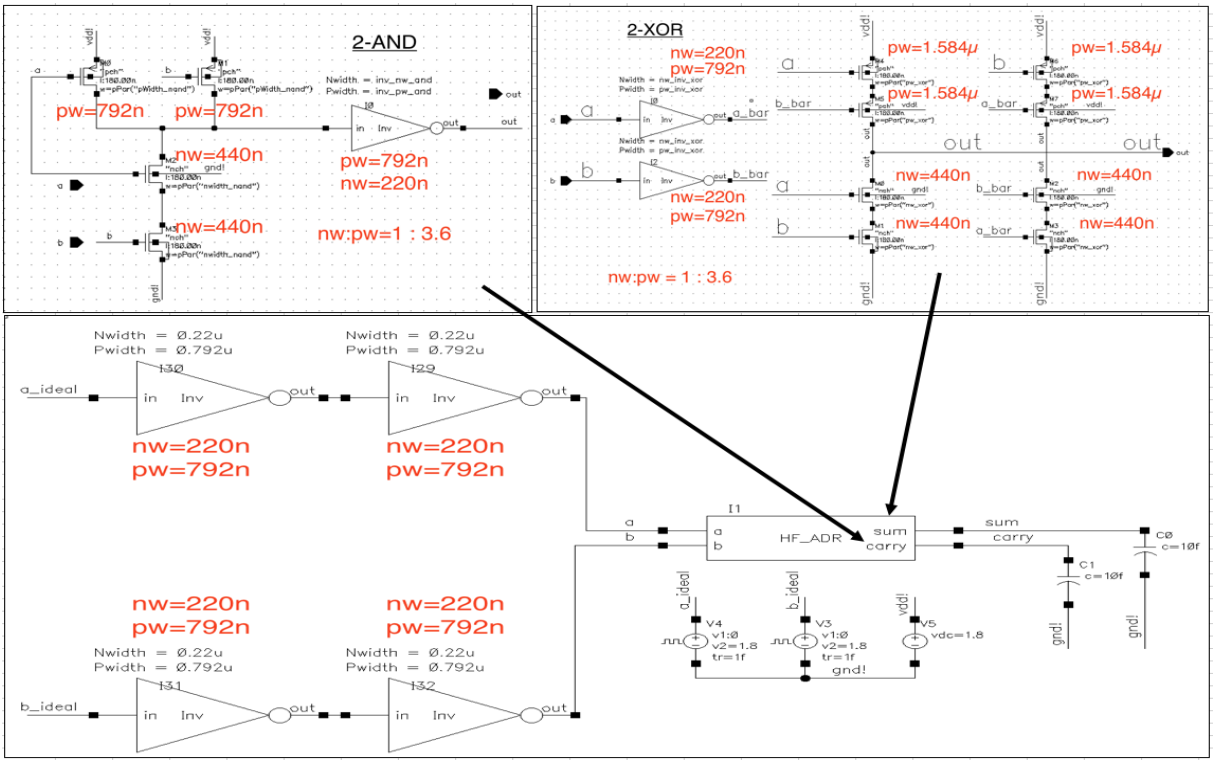

Fig. 1: Half-Adder Circuit with transistor sizing using nw:pw = 1:3.6

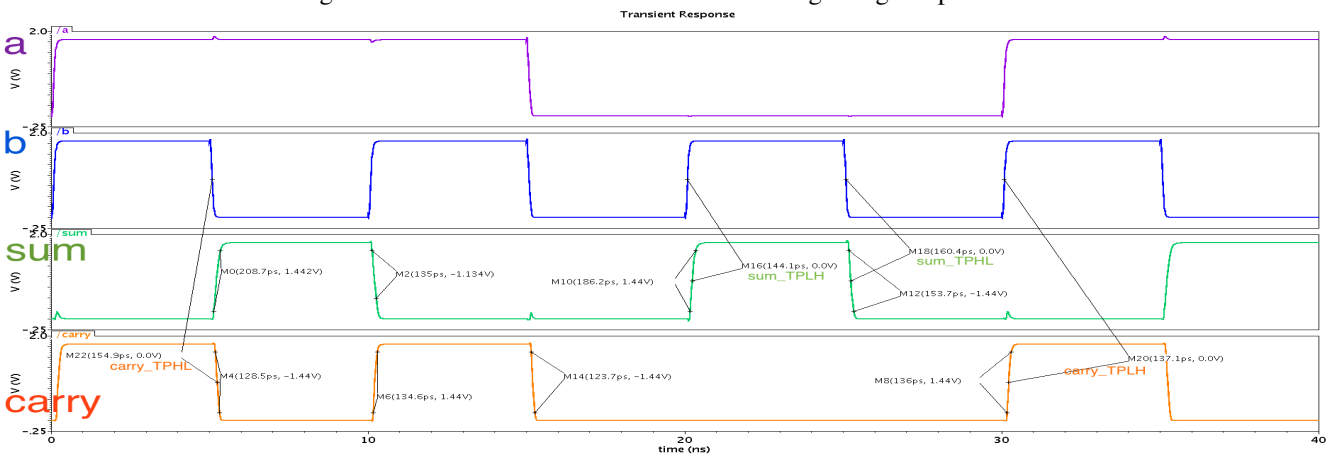

Fig. 2: Half-Adder functional timing diagram with propagation and rise/fall indicators

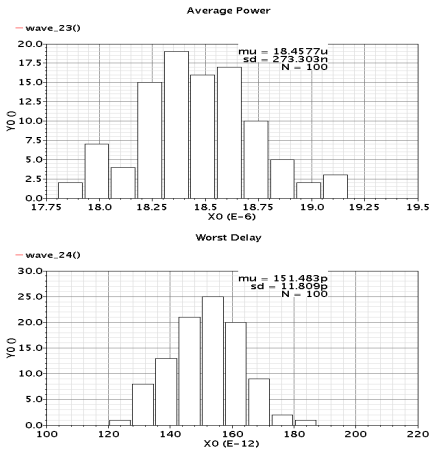

Fig. 3: Monte-Carlo simulation of 100 samples showing Worst Propagation Delay(s) and Average Power(W)

Corner	avg_pw	delay_worst	pdp
ff27	19.19u	118p	2.264f
ff85	19.67u	127.6p	2.509f
ffm25	18.85u	110.2p	2.076f
fs27	18.58u	147.9p	2.749f
fs85	18.97u	159.9p	3.034f
fsm25	18.36u	138p	2.534f
sf27	18.3u	157.6p	2.884f
sf85	18.62u	173p	3.221f
sfm25	17.99u	145p	2.609f
ss27	17.9u	196.8p	3.523f
ss85	18.18u	215.9p	3.926f
ssm25	17.74u	181.1p	3.213f
tt27	18.37u	152.3p	2.797f
tt85	18.68u	165.8p	3.097f
ttm25	18.11u	141p	2.554f

Fig. 4: Process Corner simulations for Average Power(W), Worst Propagation Delay(s), and Power Delay Product(J)