Sample-Boost-Latch Based Offset Tolerant Sense Amplifier for Subthreshold SRAMs

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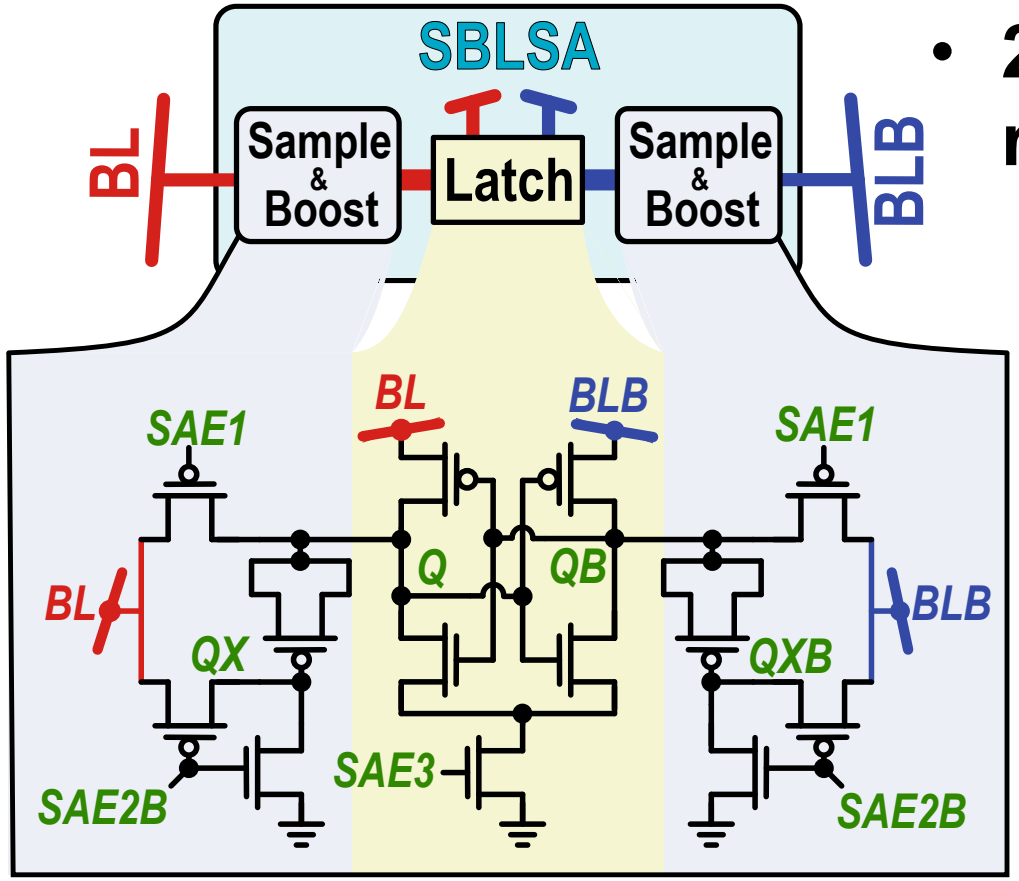
Motivation:

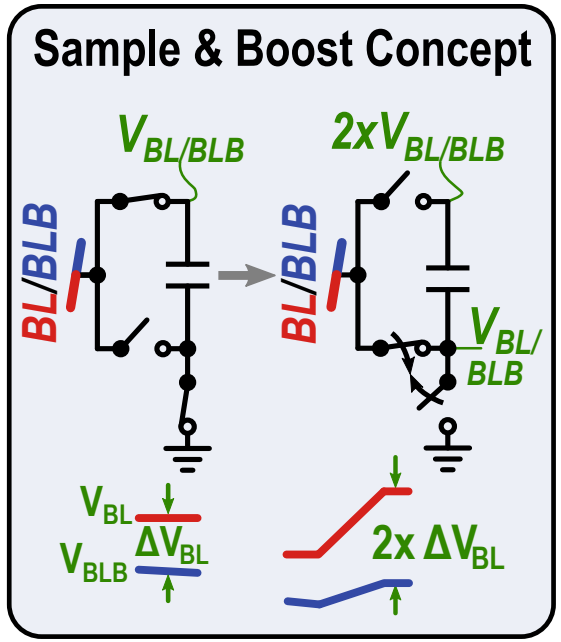
- Low-voltage, high-speed & reliable SRAMs are in high demand for SoCs
- Sense Amplifier offset play a vital role in dictating SRAM performance
- For example, for every 1 mV of Sense Amplifier offset requires ~10 mV of highly capacitive bitline discharge for 6σ SRAM yield [Abu-Rahma CICC 2011]

Sample-Boost-Latch Sense Amplifier in 65nm-GP CMOS

(1)



- $V_{DD\text{-}min}$ = 230 mV
- 23% offset reduction



(2)