Sense Amplifier Offset Characterization and Test Implications for Low-Voltage SRAMs in 65 nm

WATERLOO ENGINEERING
ELECTRICAL AND COMPUTER ENGINEERING
ece.uwaterloo.ca

Dhruv Patel, Derek Wright, Manoj Sachdev
Electrical and Computer Engineering
University of Waterloo
Waterloo, Ontario, Canada

Agenda

- **Motivation and Introduction**
  - Sense Amplifier Operation and Offset
- **Bitcell Marginal Faults and Non-Ideal Sensing**
  - Model Development and Simulation Results
- **Test Chip Design**
  - Measurement Setup and Results
  - Yield Calculation and Test Implications
- **Conclusion and Discussion**

Agenda

- **Motivation and Introduction**
  - Sense Amplifier Operation and Offset
- **Bitcell Marginal Faults and Non-Ideal Sensing**
  - Model Development and Simulation Results
- **Test Chip Design**
  - Measurement Setup and Results
  - Yield Calculation and Test Implications
- **Conclusion and Discussion**

Motivation

- SRAM SA offset is not scaling with technology
  - Crucial for memory testing and reliability

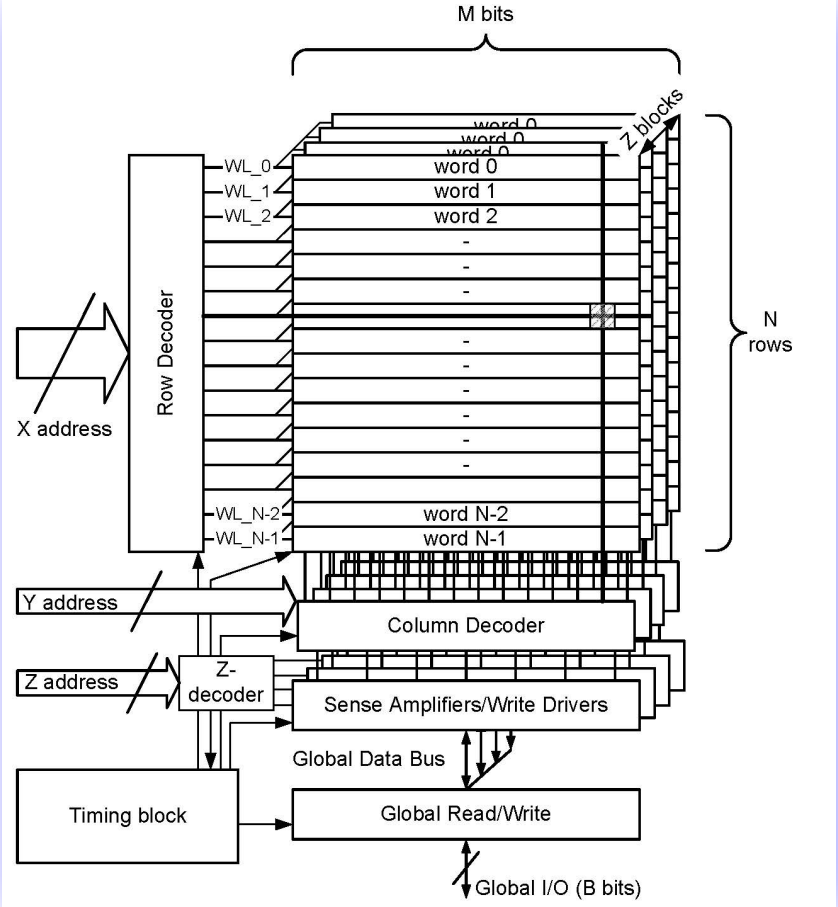
Motivation

- SRAM SA offset is not scaling with technology
  - Crucial for memory testing and reliability

To develop a parametric yield model based on SA offset, Weak cell, Column leakage

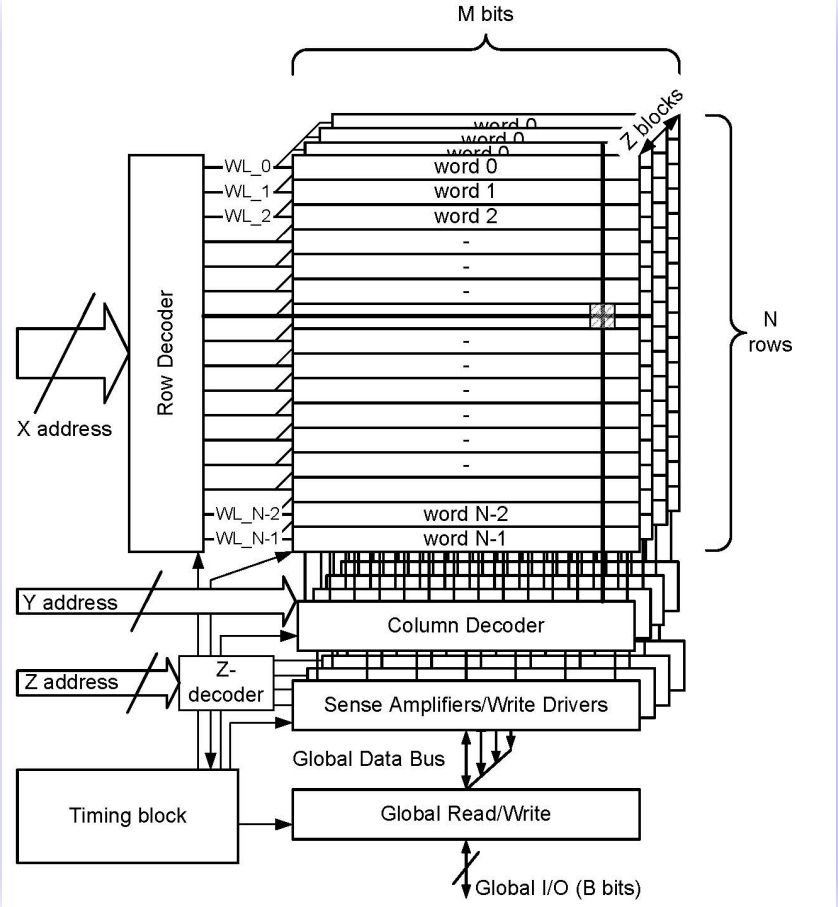
Introduction

- **SRAMs often occupy significant SoC area**
  - Contribute to quantitative & qualitative issues in SoC testing
  - March tests for quantitative test issues
  - Special DfT techniques for qualitative tests, e.g., weak cells



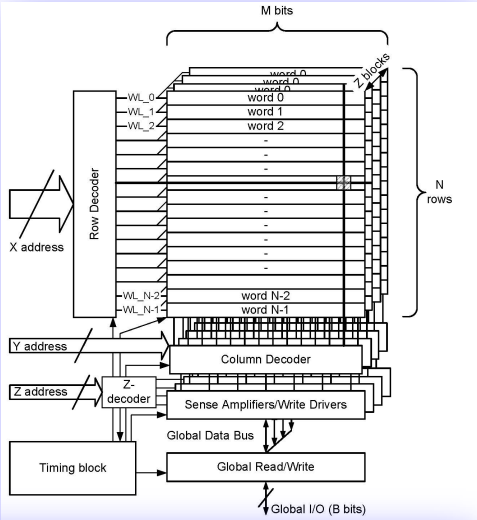
Introduction

- **SRAMs often occupy significant SoC area**
  - Contribute to quantitative & qualitative issues in SoC testing
  - March tests for quantitative test issues
  - Special DfT techniques for qualitative tests, e.g., weak cells
- **Offset voltage in SA is a known problem**
  - Results in lower yield, lower performance and is a barrier to LV SoC operation



Introduction

- **SRAMs often occupy significant SoC area**
  - Contribute to quantitative & qualitative issues in SoC testing
  - March tests for quantitative test issues
  - Special DfT techniques for qualitative tests, e.g., weak cells
- **Offset voltage in SA is a known problem**
  - Results in lower yield, lower performance and is a barrier to LV SoC operation
  - Worsening with scaling;↑process variation, ↓I_{ON}, ↑I_{OFF}



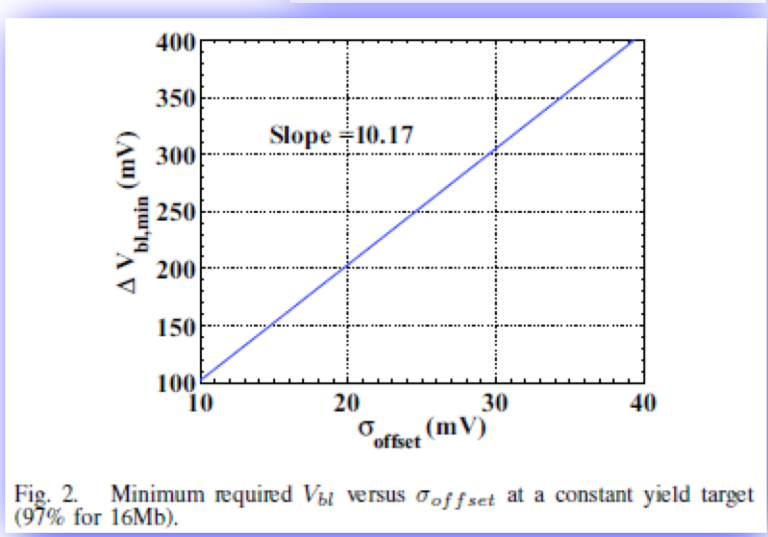
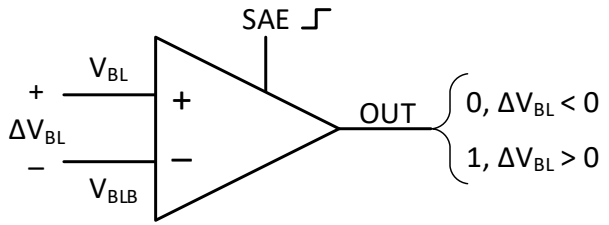


Fig. 2. Minimum required V_{bl} versus σ_{offset} at a constant yield target (97% for 16Mb).

Abu-Rahma, CICC 2011

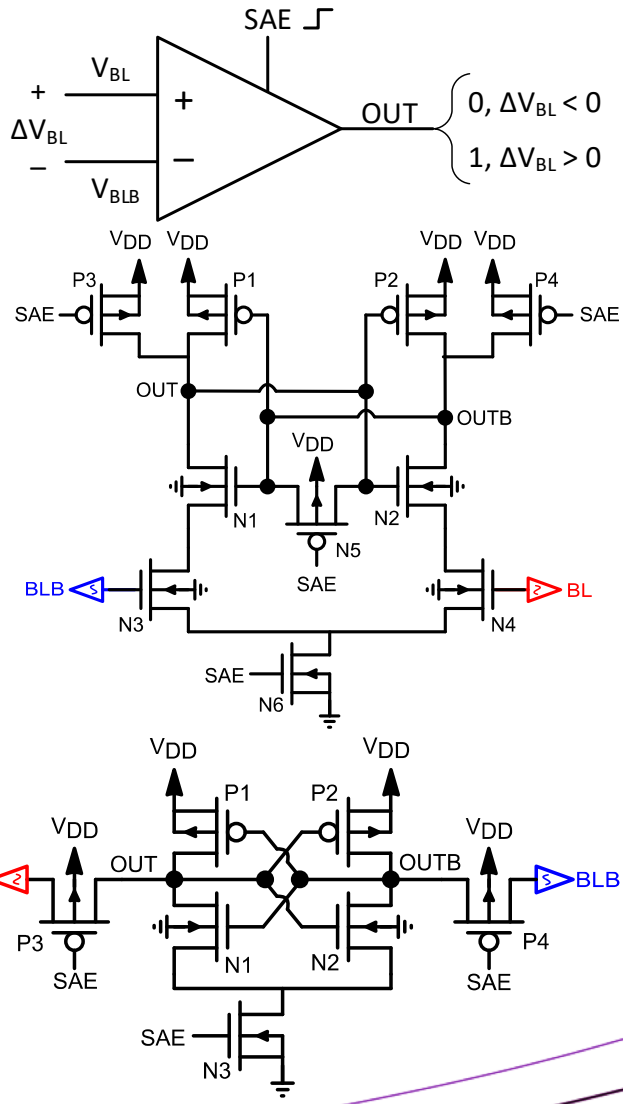
SRAM Sense Amplifiers

- **SRAM SA amplifies small differential i/p to full swing o/p**



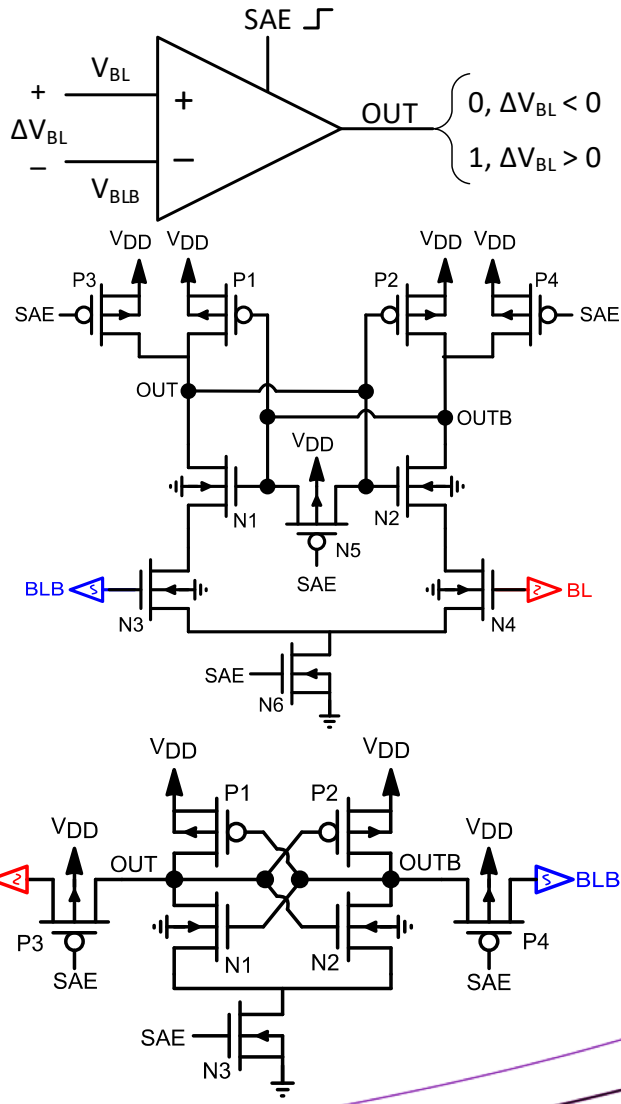
SRAM Sense Amplifiers

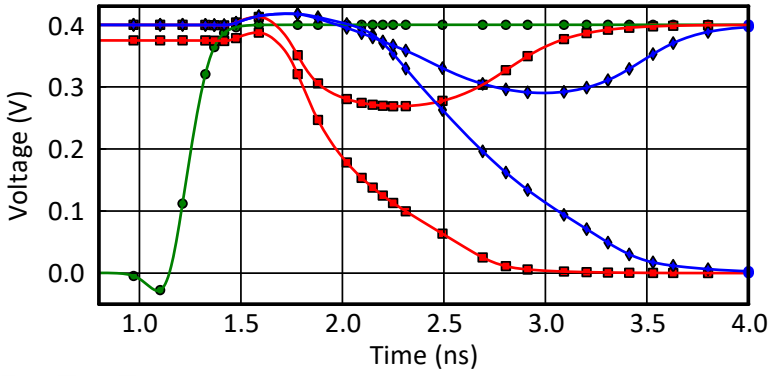
- **SRAM SA amplifies small differential i/p to full swing o/p**
  - CLSA, VLSA are popular SA configurations



SRAM Sense Amplifiers

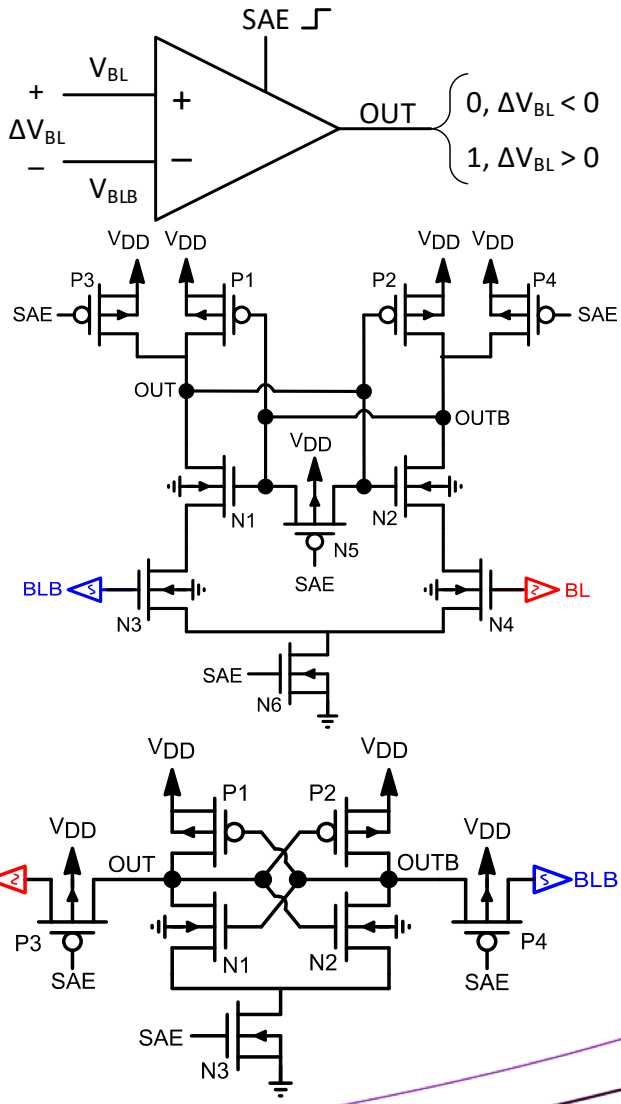
- **SRAM SA amplifies small differential i/p to full swing o/p**
  - CLSA, VLSA are popular SA configurations

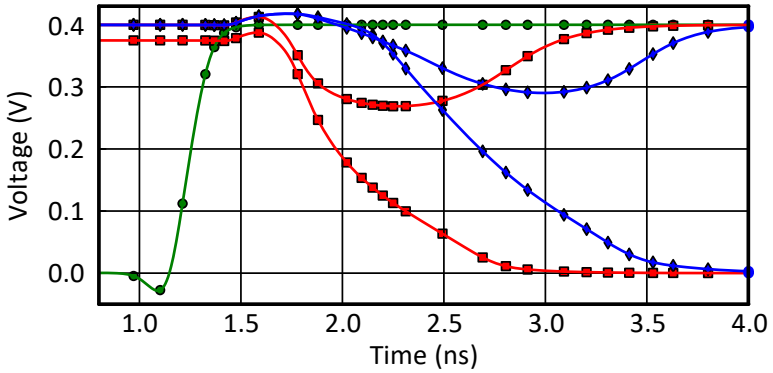




SRAM Sense Amplifiers

- **SRAM SA amplifies small differential i/p to full swing o/p**
  - CLSA, VLSA are popular SA configurations
- **V_T mismatch of the sensing transistor is the main contributor to the offset**
  - Cause for incorrect SA evaluation
  - Voltage and current mode sense amplifiers are equally affected
  - Increase in area is not a viable solution





Agenda

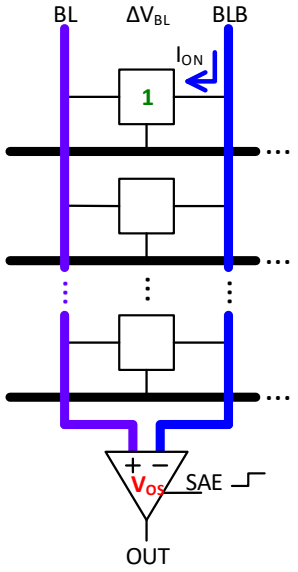
- **Motivation and Introduction**
  - Sense Amplifier Operation and Offset
- **Bitcell Marginal Faults and Non-Ideal Sensing**
  - Model Development and Simulation Results
- **Test Chip Design**
  - Measurement Setup and Results
  - Yield Calculation and Test Implications
- **Conclusion and Discussion**

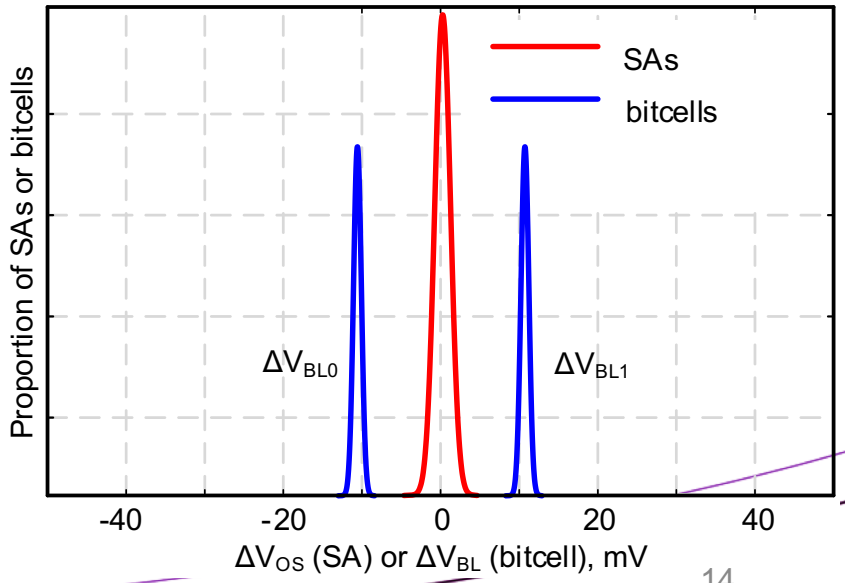
Cell Marginal Faults and SA Offset

- **I_{ON} and V_{OS} exhibit Gaussian distributions**

$$\Delta V_{BL} = \frac{I_{ON}\Delta t}{C_{BL}} \rightarrow \Delta V_{BL} \text{ has Gaussian distribution}$$

- **Normally, $\Delta V_{BL} >> \Delta V_{OS}$**





Cell Marginal Faults and SA Offset

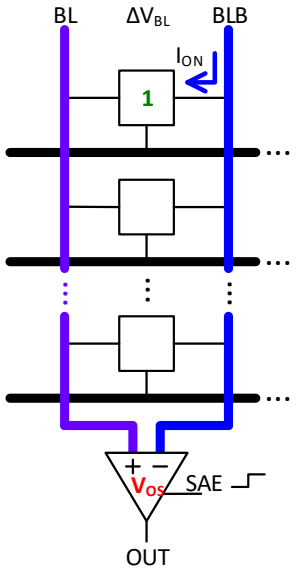
- **I_{ON} and V_{OS} exhibit Gaussian distribution**

  $\Delta V_{BL} = \frac{I_{ON}\Delta t}{C_{BL}}$ → ΔV_{BL} has Gaussian distribution

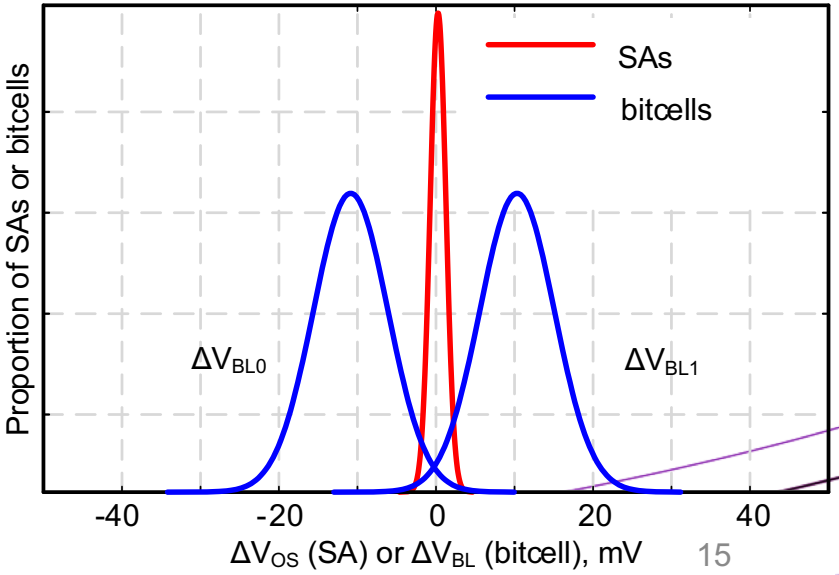
- **Normally, $\Delta V_{BL} >> \Delta V_{OS}$**

  However, finite and ↑ probability of $\Delta V_{BL} \leq \Delta V_{OS}$

  Can cause read, read stability, intermittent faults



$$f_{Y_{\Delta VBLj}}(v, \mu_{\Delta VBLj}, \sigma_{\Delta VBLj}) = \frac{1}{\sqrt{2\pi}\cdot\sigma_{\Delta VBLj}} \exp\left[-\frac{(v-\mu_{\Delta VBLj})^2}{2\sigma^2_{\Delta VBLj}}\right]$$



Cell Marginal Faults and SA Offset

- **I_{ON} and V_{OS} exhibit Gaussian distribution**

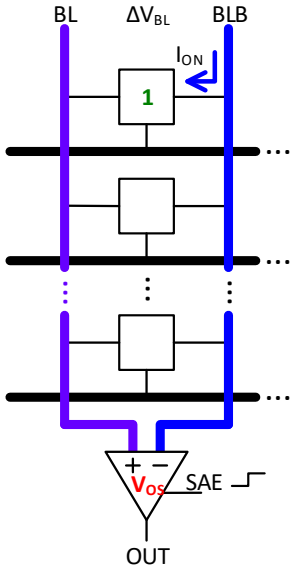
$$\Delta V_{BL} = \frac{I_{ON}\Delta t}{C_{BL}} \rightarrow \Delta V_{BL} \text{ has Gaussian distribution}$$

- **Normally, $\Delta V_{BL} >> \Delta V_{OS}$**

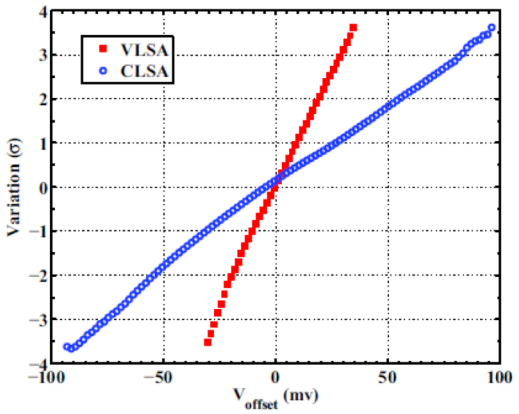
  However, finite and ↑ probability of $\Delta V_{BL} \leq \Delta V_{OS}$

  Can cause read, read stability, intermittent faults

  SA have varying V_{os}



$$f_{X_{VOS}}(v, \sigma_{VOS}) = \frac{1}{\sigma_{VOS}\sqrt{2\pi}} \exp\left(-\frac{v^2}{2\sigma_{VOS}^2}\right)$$



Abu-Rahma, CICC 2011

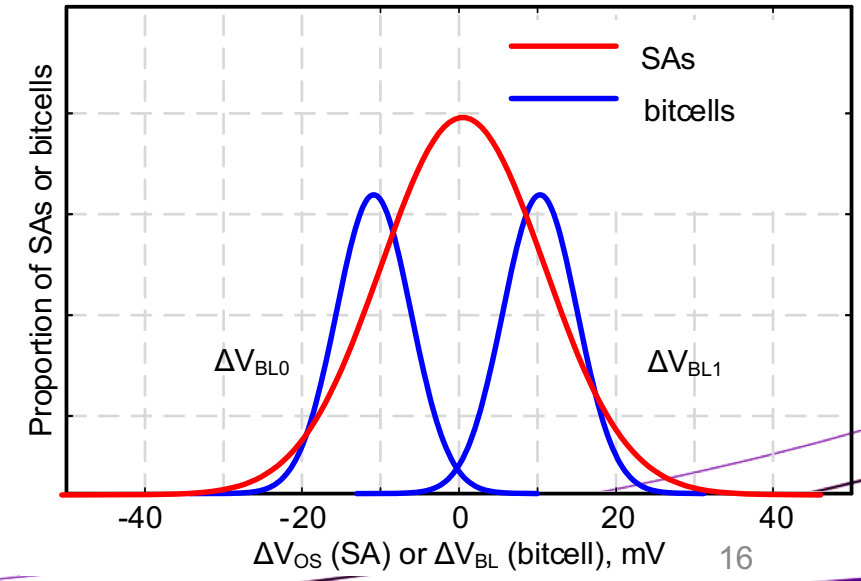
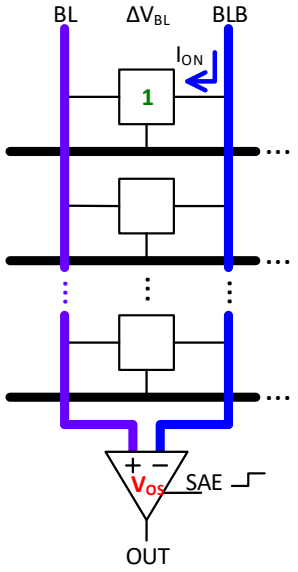


Fig. 7. Measured cumulative distribution for 35k sense amplifiers (CLSA and VLSA types of same area). The distributions follow Gaussian shape $\pm 3.5\sigma$ away from mean. Measured σ_{offset} is 9.5mV and 26.7mV for VLSA and CLSA, respectively.

Cell Marginal Faults and SA Offset - Solution



- **I_{ON} and V_{OS} exhibit Gaussian distribution**

  $\Delta V_{BL} = \frac{I_{ON}\Delta t}{C_{BL}}$ → ΔV_{BL} has Gaussian distribution

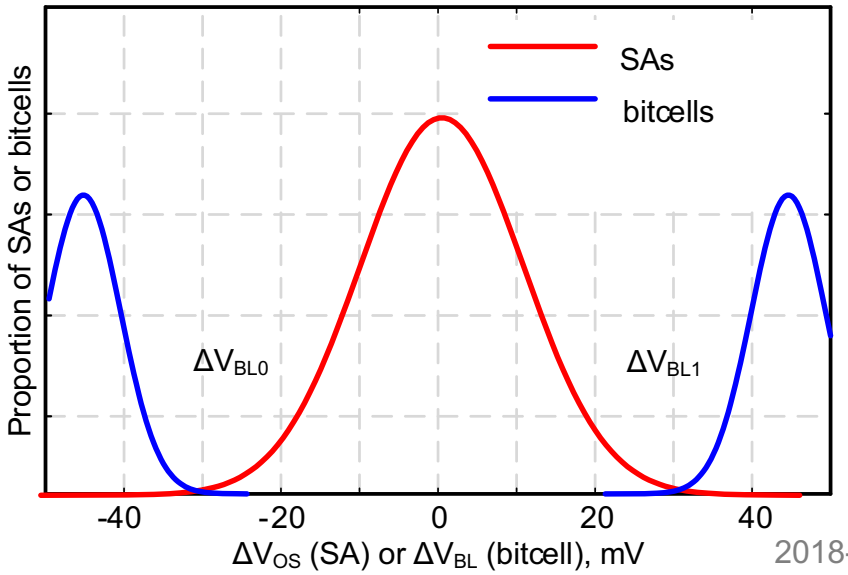
- **Normally, $\Delta V_{BL} >> \Delta V_{OS}$**

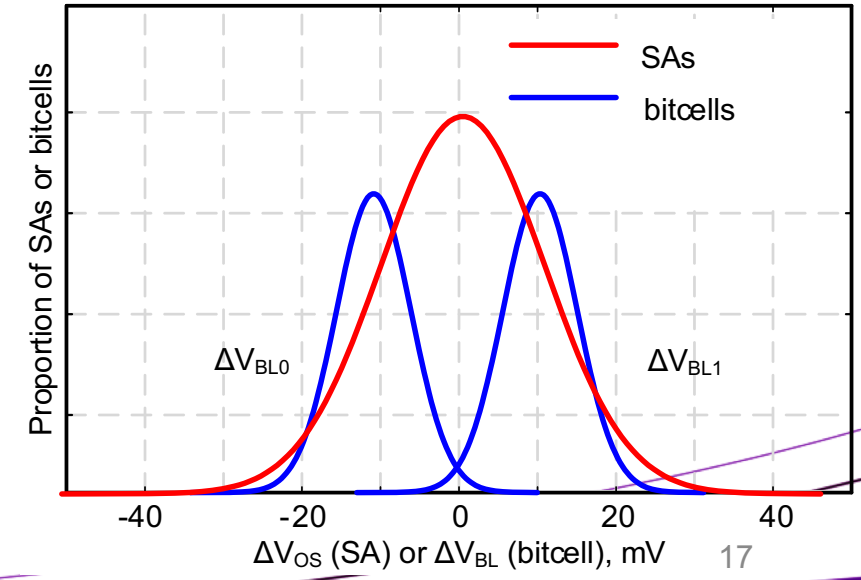
  However, finite and ↑ probability of $\Delta V_{BL} \leq \Delta V_{OS}$

  Can cause read, read stability, intermittent faults

  SA have varying V_{os}

- Increase signal development time

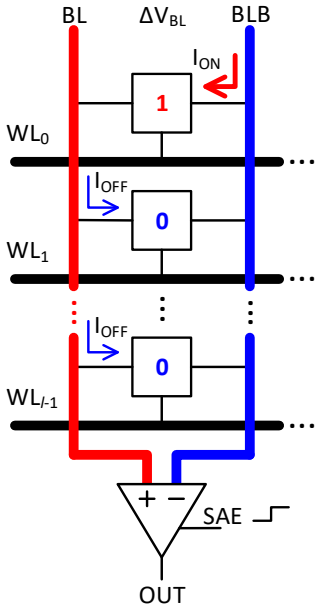




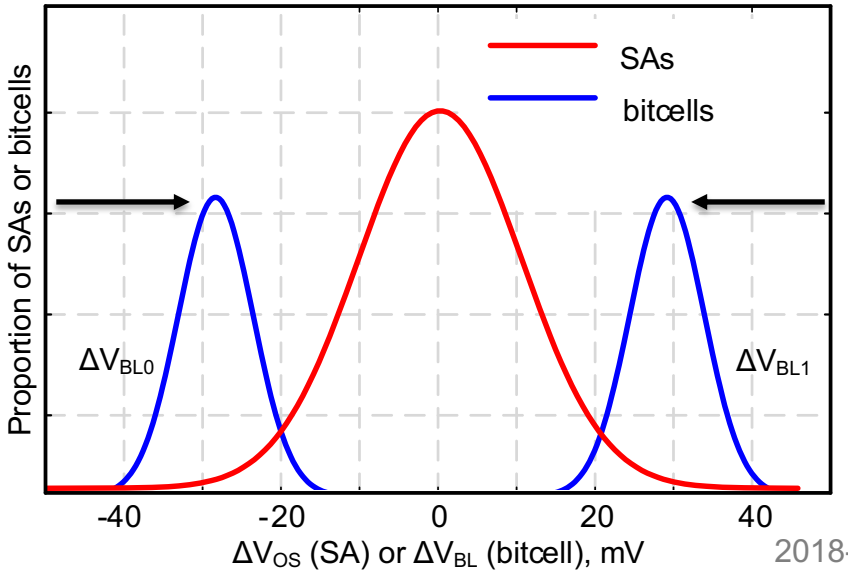
Yes, but – Leakage Current!

- **I_{OFF} from half-selected column cells can reduce ΔV_{BL}**

$$\mu_{\Delta VBL} = \frac{\Delta t[\mu_{ION} - (l-1)\mu_{IOFF}]}{lC_{BL0}}, \qquad \sigma_{\Delta VBL} = \frac{\Delta t\sqrt{\sigma_{ION}^2 + (l-1)^2\sigma_{IOFF}^2}}{lC_{BL0}}$$



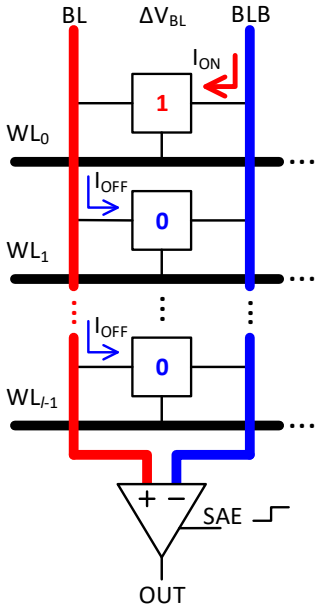
- Increase signal development time less effective
  - Can lead to intermittent, data dependent failures



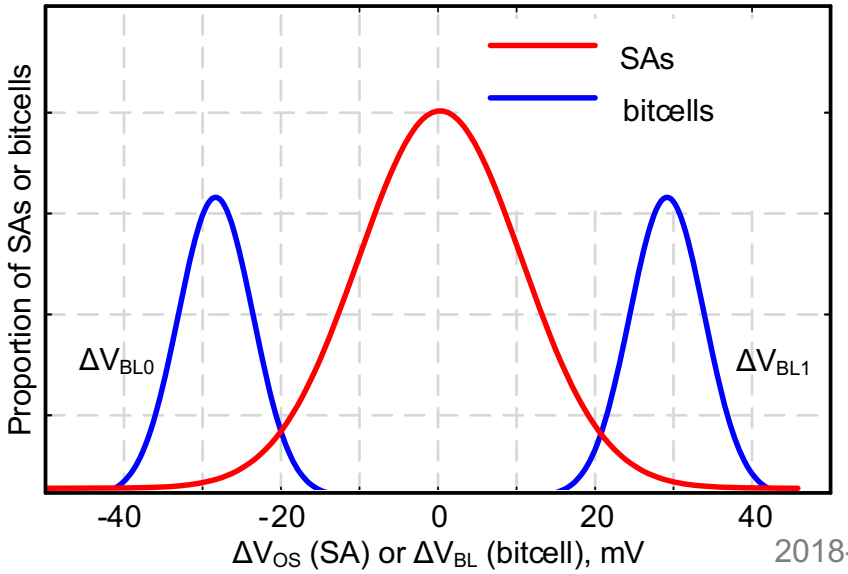
Yes, but – Leakage Current!

- **I_{OFF} from half-selected column cells can reduce ΔV_{BL}**

$$\mu_{\Delta VBL} = \frac{\Delta t[\mu_{ION} - (l-1)\mu_{IOFF}]}{lC_{BL0}}, \qquad \sigma_{\Delta VBL} = \frac{\Delta t\sqrt{\sigma_{ION}^2 + (l-1)^2\sigma_{IOFF}^2}}{lC_{BL0}}$$



- Increase signal development time does not help
  - Can lead to intermittent, data dependent failures

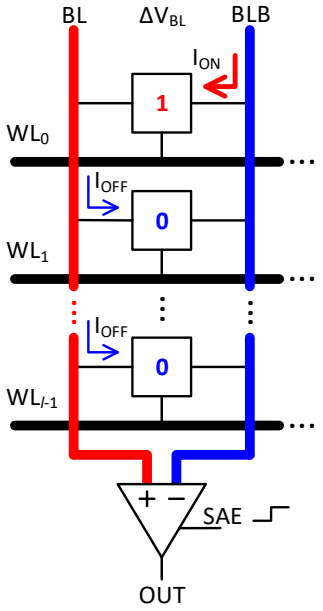


$$P_{BLF1}(v) = (\exists i)P\left(\Delta V_{BL1,i} < v\right)$$
$$= 1 - (\forall i)P\left(\Delta V_{BL1,i} \geq v\right),$$

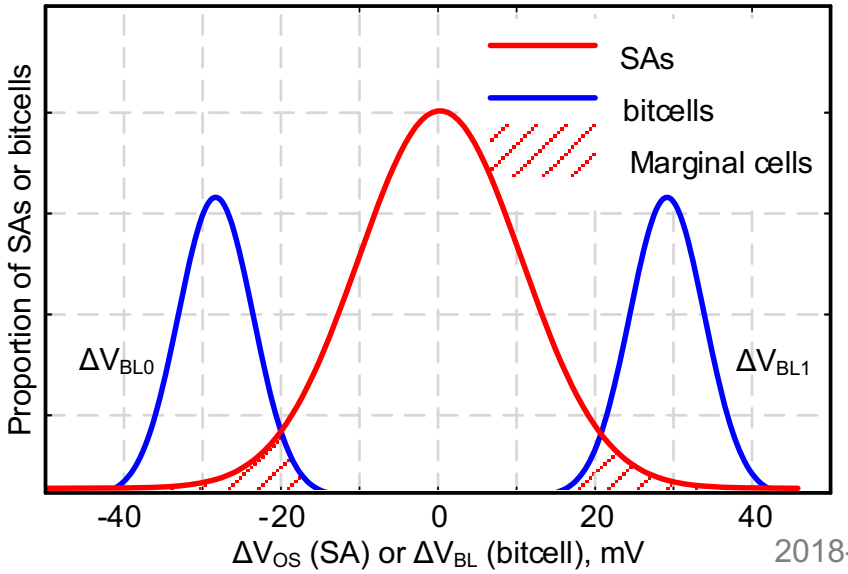
Yes, but – Leakage Current!

- **I_{OFF} from half-selected column cells can reduce ΔV_{BL}**

$$\mu_{\Delta VBL} = \frac{\Delta t[\mu_{ION} - (l-1)\mu_{IOFF}]}{lC_{BL0}}, \qquad \sigma_{\Delta VBL} = \frac{\Delta t\sqrt{\sigma_{ION}^2 + (l-1)^2\sigma_{IOFF}^2}}{lC_{BL0}}$$



- Increase signal development time does not help
  - Can lead to intermittent, data dependent failures

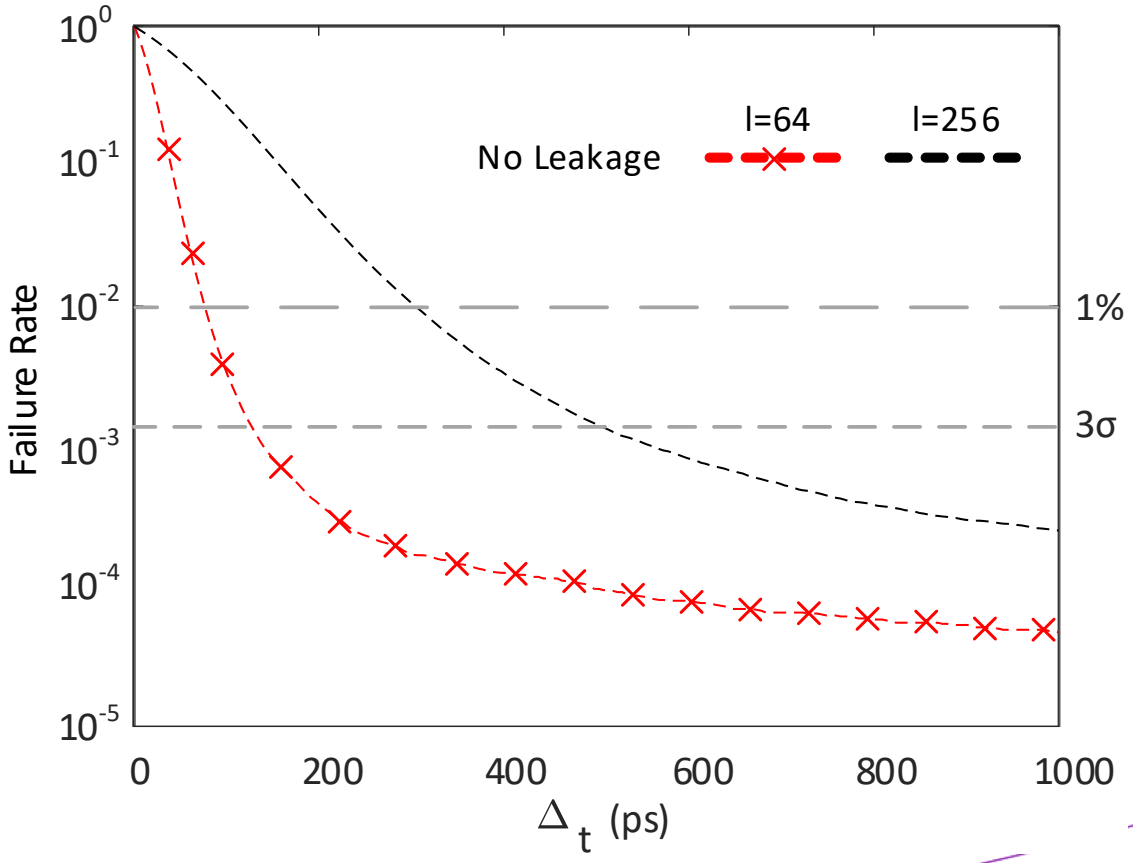


$$P_{BLF1}(v) = (\exists i)P\left(\Delta V_{BL1,i} < v\right)$$
$$= 1 - (\forall i)P\left(\Delta V_{BL1,i} \geq v\right),$$

$$P(\Delta V_{BL1} < V_{OS})$$
$$= \int_0^{V_{DD}} \int_0^{v_X} f_{X_{VOS}}(v_X) \cdot P_{BLF}(v_y)\partial v_Y \partial v_X$$

Model for Marginal Bitcell and Non-ideal SA

- Model considers V_{OS}, I_{ON}, and I_{OFF} to predict **parametric** yield
- But, we need to get model parameters from:
  - Measurement
  - Simulation

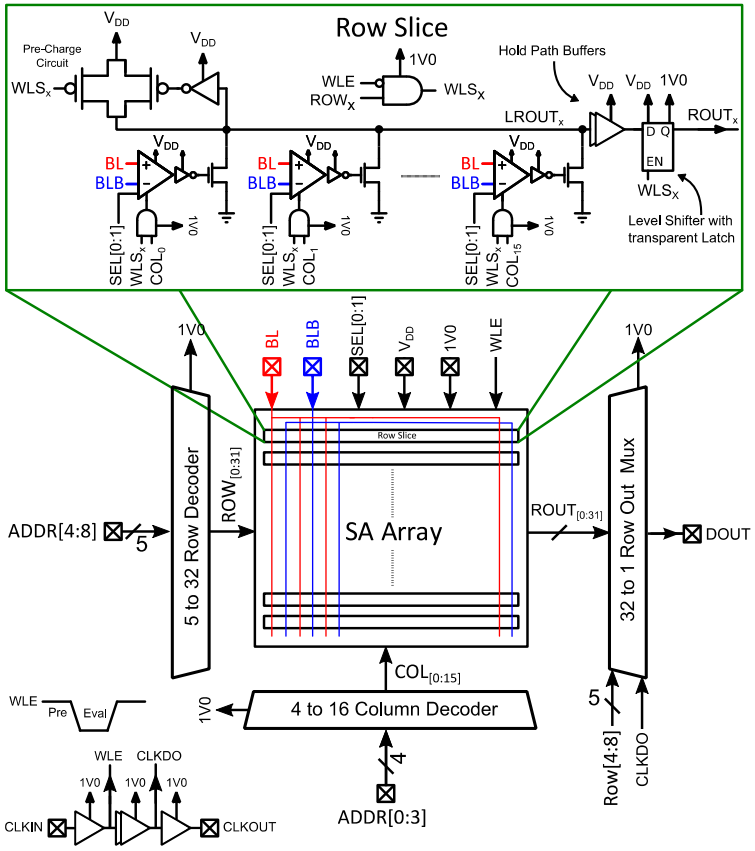


Agenda

- **Motivation and Introduction**
  - Sense Amplifier Operation and Offset
- **Bitcell Marginal Faults and Non-Ideal Sensing**
  - Model Development and Simulation Results
- **Test Chip Design**
  - Measurement Setup and Results
  - Yield Calculation and Test Implications
- **Conclusion and Discussion**

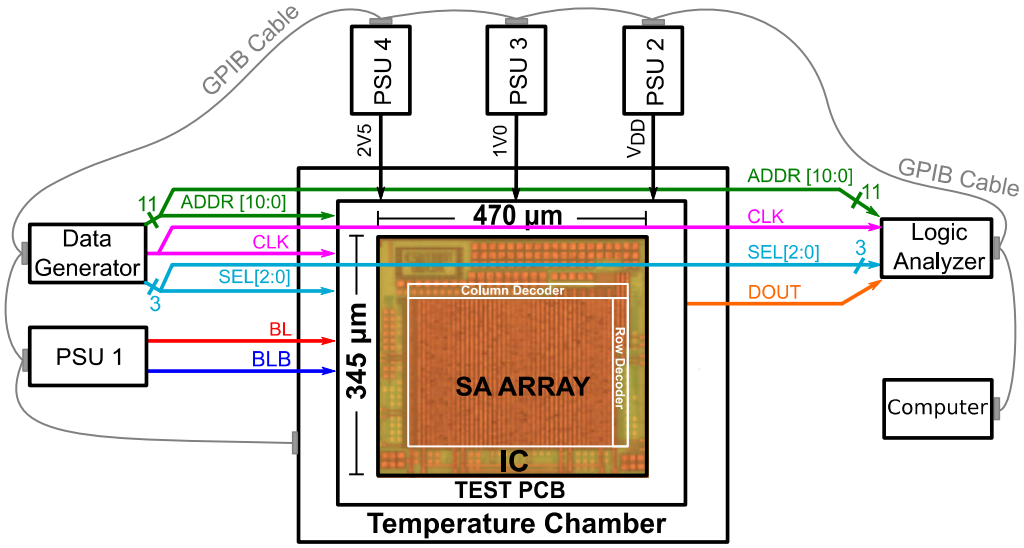
65 nm Test Chip Design, Measurement Setup

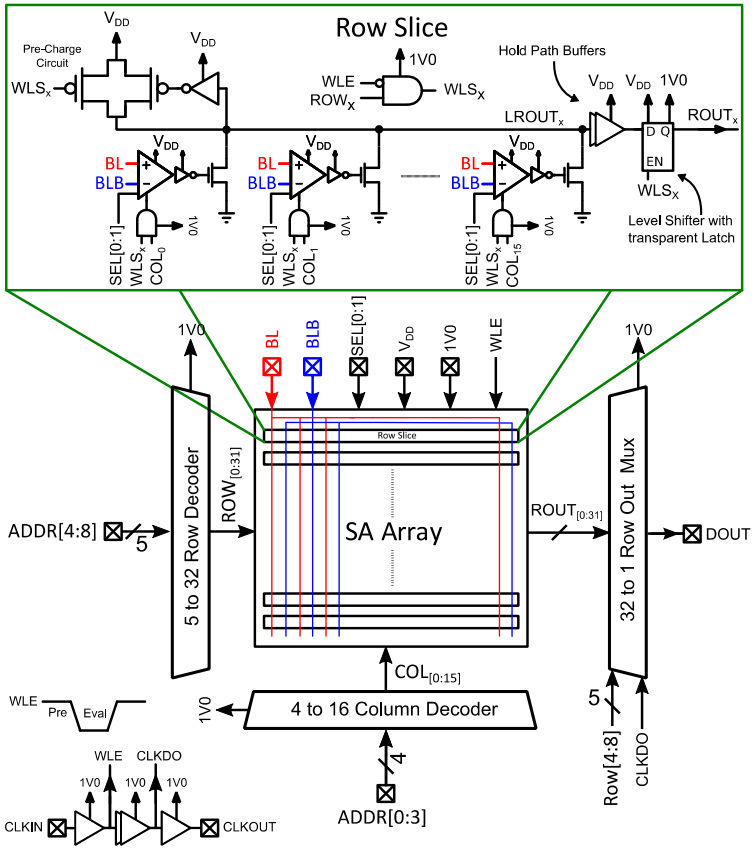
- **Arrays 32x16 VLSAs & CLSAs**
  - Each SA individually addressed
  - ΔV_{BL} is driven by input pads with 1 mV step



65 nm Test Chip Design, Measurement Setup

- **Arrays 32x16 VLSAs & CLSAs**
  - Each SA individually addressed
  - ΔV_{BL} is driven by input pads with 1 mV step

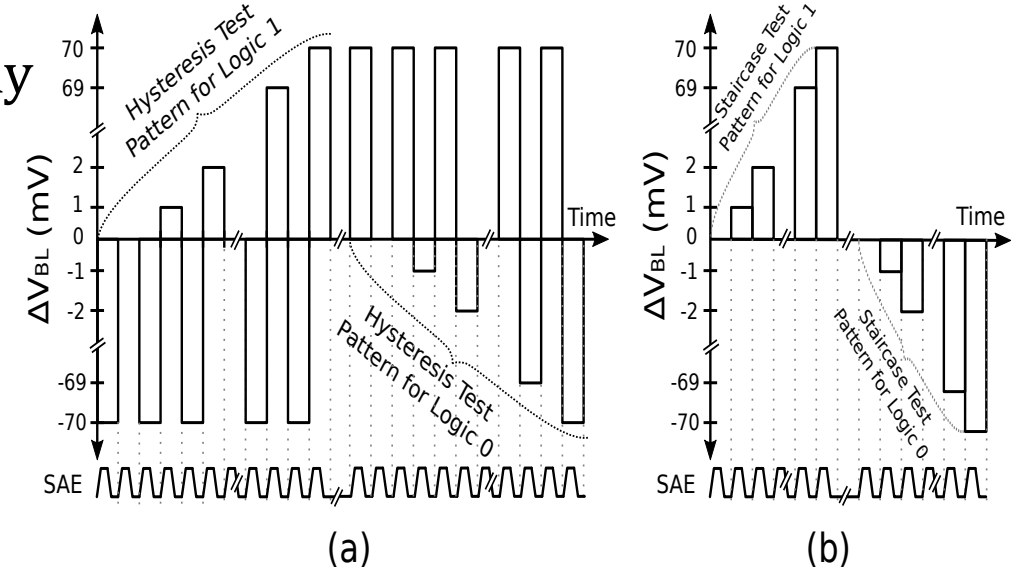




- **Measurement setup**
  - V_{DD}, CLK, BL, BLB, A[0-8] externally supplied
  - Thermal chamber
  - Data is captured by LA; and processed

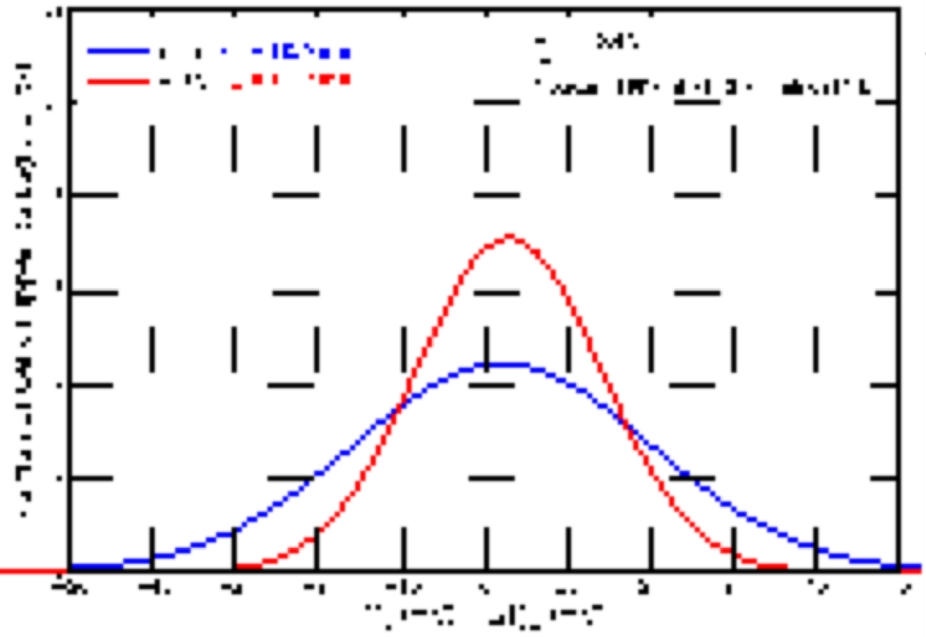
Test Stimuli, Measurement Results

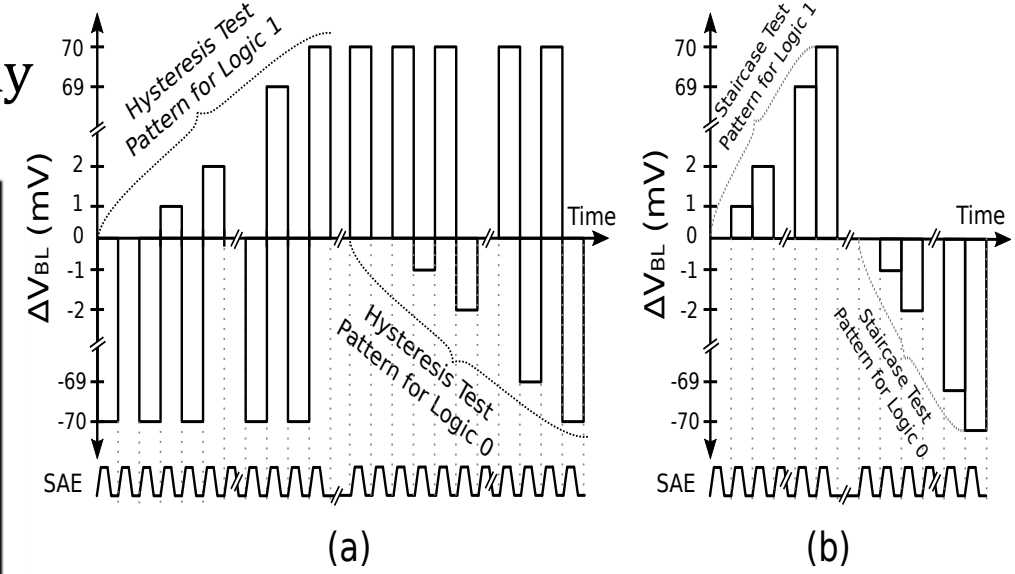
- **Hysteresis and Staircase patterns to discount potential SA memory effect**
  - ΔV_{BL} is increased successively



Test Stimuli, Measurement Results

- **Hysteresis and Staircase patterns to discount potential SA memory effect**
  - ΔV_{BL} is increased successively



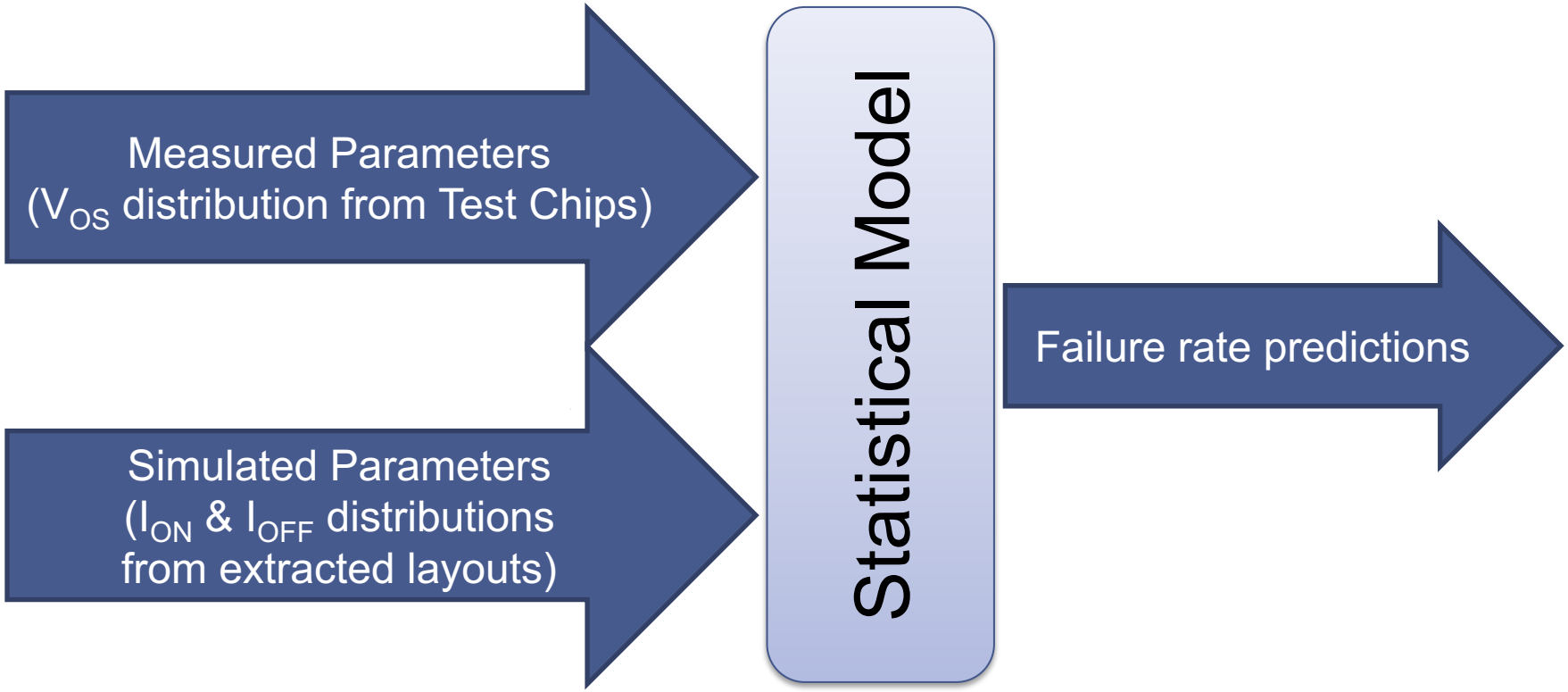


- **Measurement results**
  - 512x10 CLSAs and VLSAs

$\sigma_{os\text{-}VLSA} = 11$ mV

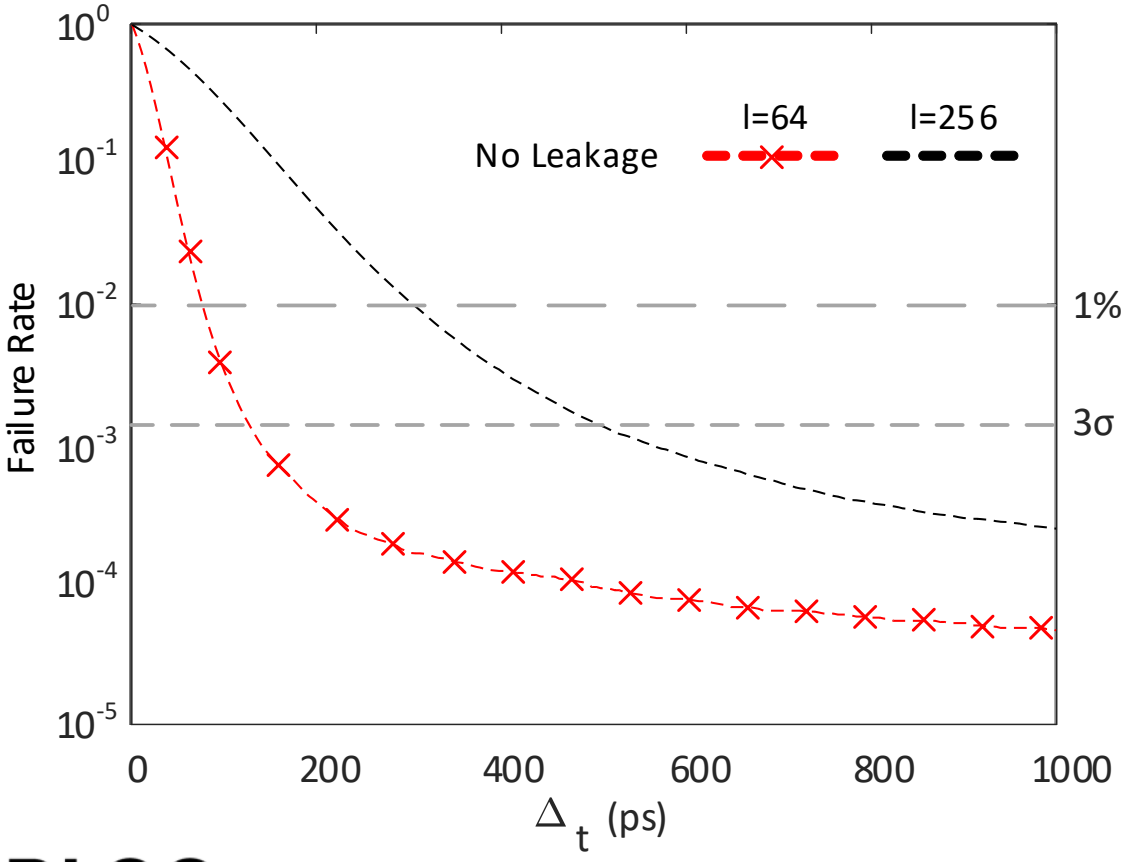
$\sigma_{os\text{-}CLSA} = 18$ mV

Improved Model Parameters



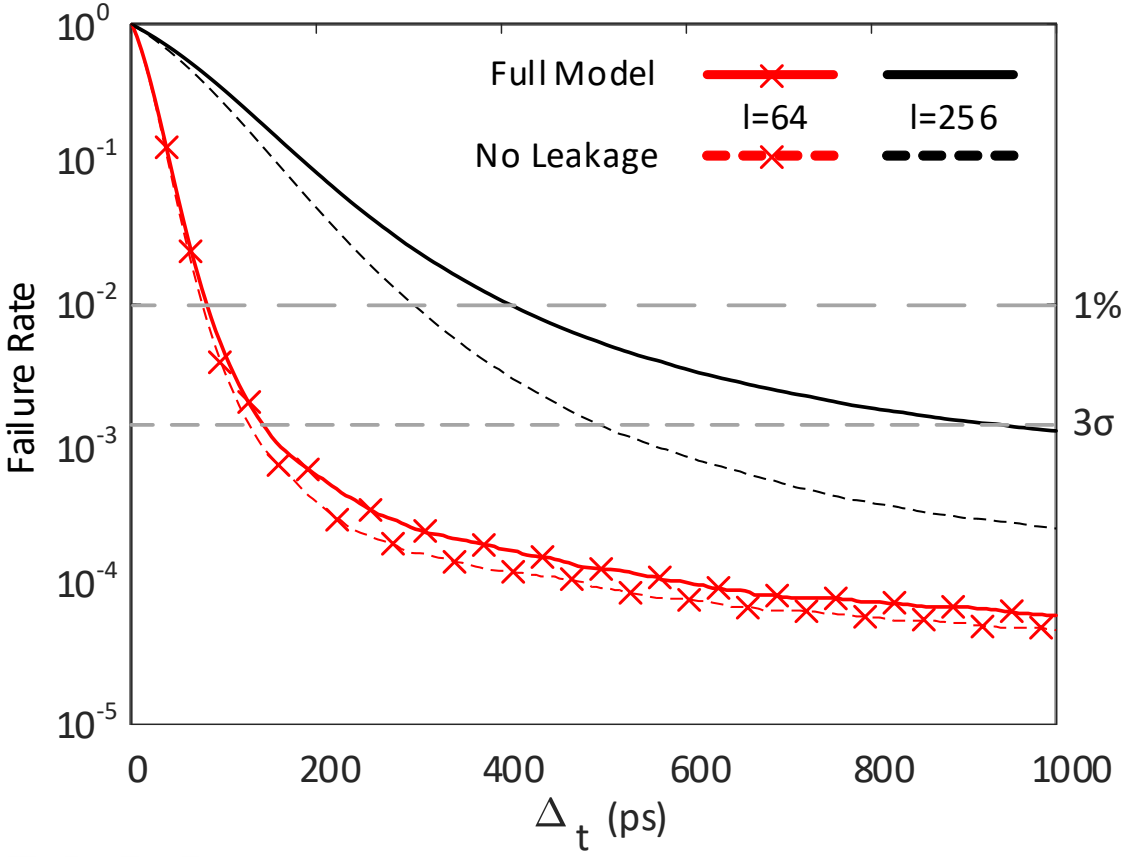
Model for Marginal Bitcell and non-ideal SA

- Model takes into consideration V_{os}, I_{ON}, and I_{OFF} to predict **parametric** yield



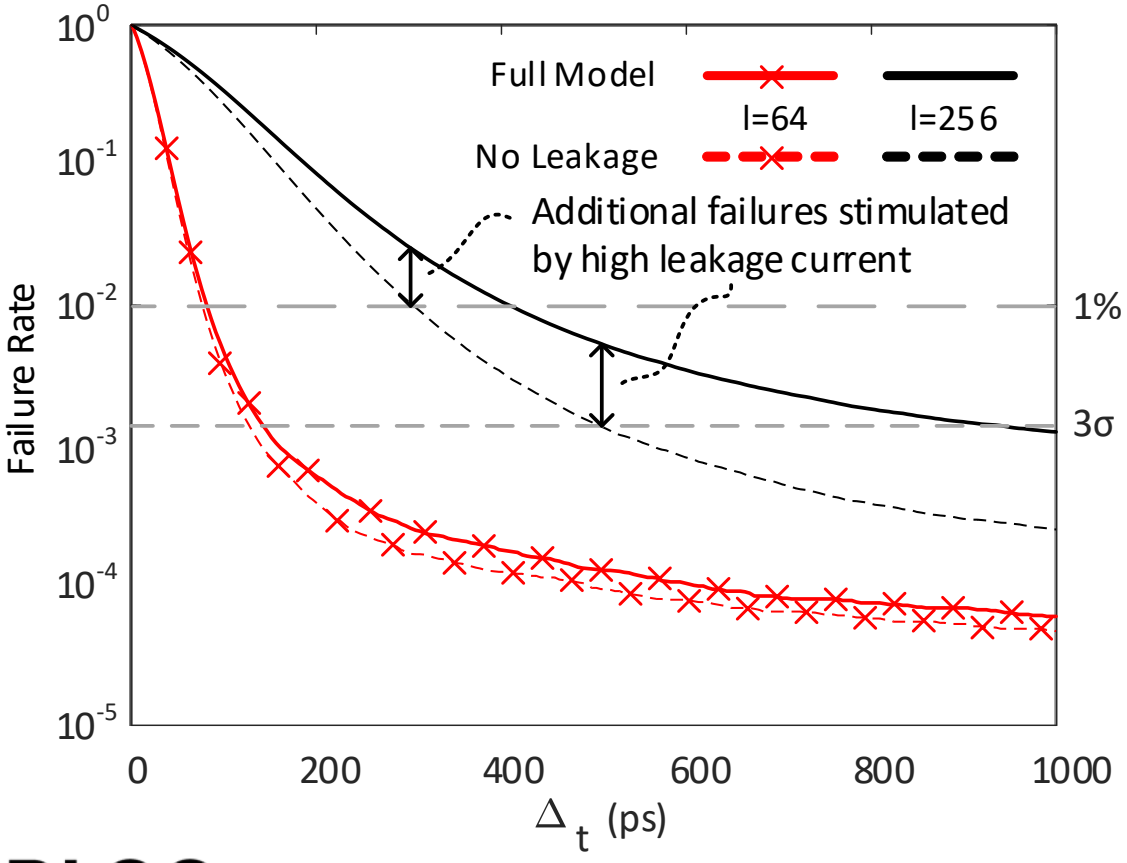
Model for Marginal Bitcell and non-ideal SA

- Model takes into consideration V_{os}, I_{ON}, and I_{OFF} to predict **parametric** yield



Model for Marginal Bitcell and non-ideal SA

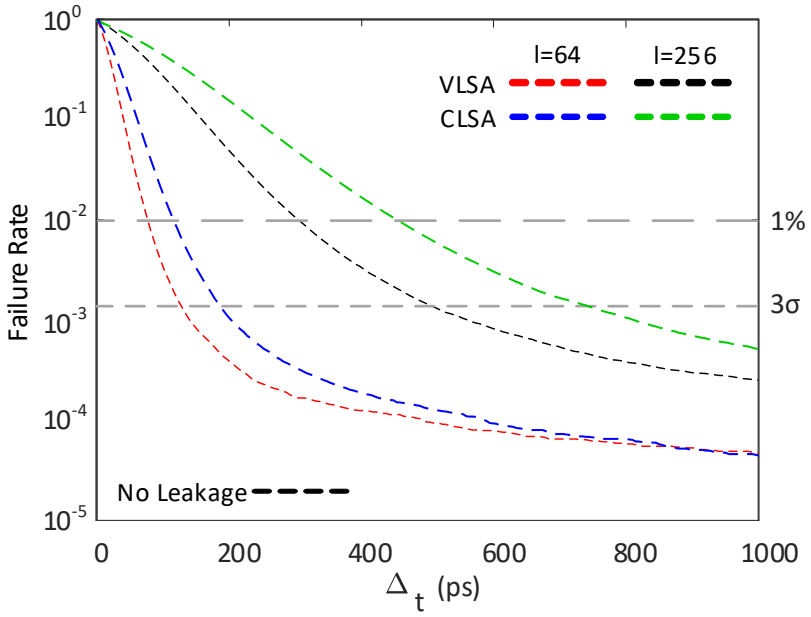
- Model takes into consideration V_{os}, I_{ON}, and I_{OFF} to predict **parametric** yield



SA Offset – CLSA vs. VLSA

- **SA offset from testchip is included in the model**

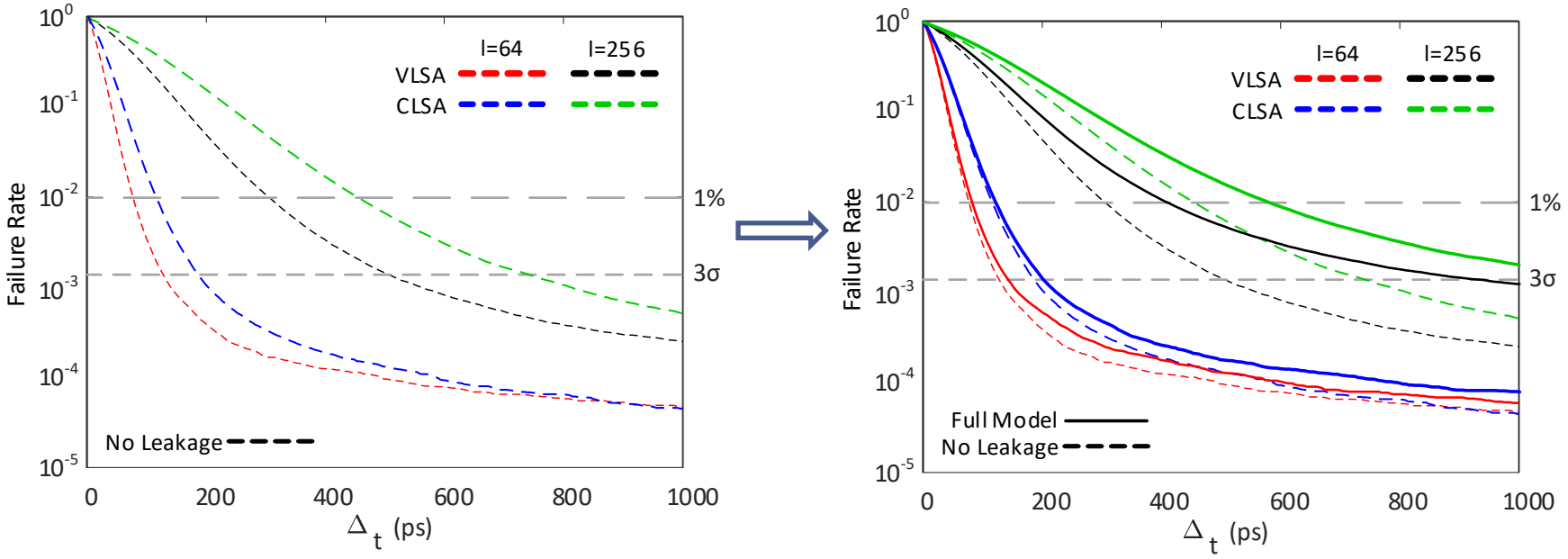
  $\sigma_{os\text{-}VLSA} = 11$ mV; $\sigma_{os\text{-}CLSA} = 18$ mV



SA Offset – CLSA vs. VLSA

- **SA offset from testchip is included in the model**

  $\sigma_{os\text{-}VLSA} = 11$ mV; $\sigma_{os\text{-}CLSA} = 18$ mV



Model suggest increased $\sigma_{os\text{-}CLSA}$ contributes increased parametric yield loss

Test Implications

- Worst case for testing SA offset and weak cells
  - Lower V_{DD}, higher temperature
- Half selected column cell leakage can help in providing debug/diagnostic resolution between SA offset and weak cell failures

Agenda

- **Motivation and Introduction**
  - Sense Amplifier Operation and Offset
- **Bitcell Marginal Faults and Non-Ideal Sensing**
  - Model Development and Simulation Results
- **Test Chip Design**
  - Measurement Setup and Results
  - Yield Calculation and Test Implications
- **Conclusion and Discussion**

Concluding remarks

- Sense Amplifier offset is an impediment to LV, LP SRAM operation
- A parametric yield model based on SA offset, column leakage, temperature is developed
  - Model is able to provide debug resolution between SA offset and weak cells
- Future work
  - Impact of timing, power supply noise